

New Three-Phase Symmetrical Multilevel Voltage Source Inverter

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Abstract—This paper presents a new design and implementation of a three-phase multilevel inverter (*MLI*) for distributed power generation system using low frequency modulation and sinusoidal pulse width modulation (*SPWM*) as well. It is a modular type and it can be extended for extra number of output voltage levels by adding additional modular stages. The impact of the proposed topology is its proficiency to maximize the number of voltage levels using a reduced number of isolated dc voltage sources and electronic switches. Moreover, this paper proposes a significant factor ($F_{C/L}$), which is developed to define the number of the required components per pole voltage level. A detailed comparison based on $F_{C/L}$ is provided in order to categorize the different topologies of the *MLIs* addressed in the literature. In addition, a prototype has been developed and tested for various modulation indexes to verify the control technique and performance of the topology. Experimental results show a well-matching and good similarity with the simulation results.

Index Terms—Low frequency modulation, multi-level inverter, multi-level inverter comparison factor, sinusoidal pulse-width modulation (*SPWM*), symmetrical DC power sources, three-phase.

NOMENCLATURES

$F_{C/L}$	Components per pole voltage level.
N_{Pole}	Number of voltage levels per pole.
N_C	Capacitors count.
N_D	Diodes count.
N_{SW}	Switching devices count.
N_{PS}	dc-power supplies count.
N_{tsf}	Transformers count.
N_X	Other additionally components count.

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M_{Level}	Number of output line-to-line voltage levels.
N_{Ph}	Number of output phase voltage levels.
N_{Cell}	Number of the used basic cells per arm.

I. INTRODUCTION

RECENTLY, multi-level inverters (*MLIs*) have obtained great attention as a single stage inverter. Although, they need high number of components, but due to their advantages such as generating output voltage with extremely low distortion factor (*DS*), low dv/dt , small output filter size, low electro-magnetic interface (*EMI*), and low total harmonic distortion (*THD*), *MLIs* still have great attention [1]–[6]. Practically, all of these advantages appear strongly as the number of dc-power sources increased as in the case of renewable energy systems.

The general concept of *MLIs* is to utilize isolated dc sources or a bank of series capacitors to produce ac voltage waveforms with higher amplitude and near sinusoidal waveform. There are three conventional types of *MLIs* named as neutral point diode clamped (*NPC*) *MLI* [7], flying capacitor (*FC*) *MLI* [8], and cascaded H-Bridge (*CHB*) *MLI* [9]. Almost all of them are suffering from increased components number per level, and complex control architecture [9].

Among the different topologies for *MLIs*, they can be classified into two main categories: 1) single dc-source inverter such as *FC*, and *NPC* inverters; 2) multi-dc sources inverters such as *CHB* inverter [10]. While, multi-dc sources inverter is divided into symmetrical and nonsymmetrical topologies. Principally, nonsymmetrical topologies produce more voltage levels compared to symmetrical topologies. Almost all of these topologies can be extended for more voltage levels by increasing the number of the primary configuration (basic cell).

Many topologies were presented in the last decade focusing on minimizing the basic multilevel topologies drawbacks. The author in [11] presented a topology named multilevel dc link (*MLDCL*). It consists of a group of basic cells connected in series configuration. Each cell produces E or 0 voltage across the connected cells, there is an H-bridge to change the polarity of the synthesized voltage. The required number of active switches for (m) output voltage levels is ($m + 3$) for the *MLDCL* inverters. However, this topology requires increased number of components compared to the conventional topologies, and high voltage stresses.

However, in [12], the authors presented a topology named transistor-clamped H-bridge (*TCHB*). The primary cell

can produce a five-levels per pole in the output voltage ($\pm E, \pm(1/2)E, 0$). However, it suffers also from the increased components counts, requirements of electrolytic capacitors, complex control methodology.

On the other hand, in [13], the authors presented three-phase asymmetrical multi-level cascade inverter. The output voltage levels synthesized by series connected cells like in [11]. For two cells configuration, it produces four levels per pole ($0, E, 2E, 3E$). However, instead of using H-bridge to getting the opposite voltage polarities as in [11], it uses simply the phase shift relationship between the three legs, by subtracts each leg's voltage with the neighboring one to produce the line voltage, the same subtraction idea was presented in [14].

While, the authors in [15] presented a new single dc-link power supply topology, the presented topology generates seventeen voltage levels ($0, E/16, E/8, 3E/16, E/4, 5E/16, 3E/8, 7E/16, E/2, 9E/16, 5E/8, 11E/16, 3E/4, 13E/16, 7E/8, 15E/16$ and E) on the output voltage by using three level flying capacitor inverter and cascades H-bridge. However, this topology utilizes a single dc-power supply. It uses increased number of electrolytic capacitors as floating dc-power supplies. The authors in [16] presented a double sub-module circuit. The presented cell generates a three output voltage levels across its terminals using eight switches and two capacitors. It improved the voltage balancing over capacitors at low switching frequencies, however an extra components compared with the equivalent half bridge modules required.

Some topologies such as in [17] were presented for large-scale application. They basically use a dc-ac inverter stage to convert the dc output voltage from the PV modules to the required ac-voltages. That in turns transformed into three ac isolated voltages using a medium frequency transformer having three secondary windings. This configuration suffers from many limitations like increasing components counts, high cost, *EMI* noise, low efficiency, and big installation size.

Based on a nested arrangement, a new sub-family of *MLIs* was presented in [18]. The nested *MLIs* actually lay in multi dc-power sources topologies category. They have two configurations; one produces an odd number of output voltage levels and the other is belonging to even number of output voltage levels. In order to generate a four voltage levels, it requires three dc-power supplies, four capacitors, and 18 switches. However, it has no diodes compared to the *NPC* inverters but it requires two extra dc-power supplies. Besides, it uses electrolytic capacitors that has increased the system cost and size.

In [19], a hybrid cascaded inverter was presented. Its operation depends on constructing unidirectional staircases waveforms generated from a series connected cells. Each cell consists of one capacitor and four switching devices. Although this topology uses only one single dc-source, but it has many limitations due to capacitors, existence of three-phase transformer, and high voltage stress on the H-bridge switches as the number of levels is increased.

In [20], the authors presented a modified flying capacitors topology; it requires three dc-power supplies, nine capacitors, and 36 switching devices to produce five levels for pole voltages. It suffers from the same limitation founded in [15] and capacitor's voltage balancing problems.

In [21], [22] different basic cells were presented named as clamp-double cell. In order to generate three voltage levels, it requires five switches, two capacitors and two diodes. Compared to the half and full-bridge inverters, it has higher semiconductor losses than the half-bridge inverter [23]. Another basic cell is named five-level cross-connected circuit was presented in [22]. It generates five output voltage levels. However, it requires six switching devices and two capacitors for its operation. Modified cells were created by combining common known basic cells such as half bridge, full bridge, that can be connected in series, in parallel, in cascaded, or in cross configurations. The resulting cells aim to overcome the basic cells drawbacks. The resulting cells are classified as mixed commutation cells, asymmetrical commutation cells, cross-connected commutation cells, clamped double commutation cells, and T-connected *NPC*. However, all of them suffer from electrolytic capacitor limitations.

In [24]–[27], new sub-families of the *MLI* were produced. They mainly consist of a high voltage main stage linked with low voltage auxiliary stages. The main stage commonly utilizes a conventional voltage source inverter or *NPC*-three level inverter. It has high voltage single dc-power supply and auxiliary cascaded cells either are a full H-bridge or half H-bridge cells. Almost these topologies are suitable in medium voltage applications. It has low components counts as isolated dc-power supplies and switches. Nevertheless, it seems to have a high conduction loss since a zero voltage state in the pole requires ' n ' switches (for half H-bridge) or ' $2n$ ' (for full H-bridge) be in ON-state.

Obviously, from the above survey, there are many different topologies for *MLIs*. Some of them use single dc-power supply and others use many dc-power supply s. In addition, some of them use many electrolytic capacitors as floating power supplies and some of them not. Almost all of addressed topologies suffering from increased number of components counts and usage of electrolytic capacitors as floating power sources which add more complicated problems in the control system. On the other hand, introducing new topology that can solve the stated challenges and proposing new factor for distinguishing different topologies are highly recommended. This paper is tackling to reduce the components count compared with the conventional and the addressed *MLIs* topologies in the literature with keeping the same pole voltage levels number. This leads to reduced inverter size, minimized switching losses, low conduction losses, and simple control architecture.

In addition, a comparison strategy based on components per level factor ($F_{C/L}$) has been proposed in this paper. This factor is used to define the required components to produce one voltage level across the output pole. Therefore, it acts as a comparison tool that is describing how the different topologies of *MLIs* fully utilize their components. This factor is defined in (1). If this factor ($F_{C/L}$) has a high value, this indicates that a large number of components counts is required to produce one pole voltage level and vice versa. Therefore, the research target is to decrease this factor

$$F_{C/L} = \frac{N_C + N_D + N_{SW} + N_{PS} + N_{tsf} + N_X}{N_{Pole}}. \quad (1)$$

TABLE I
MLI TOPOLOGIES COMPARISON

Presented in		N_{Pole}	N_{PS}	N_{SW}	N_D	N_C	N_{tsf}	$F_{C/L}$
[11]		3	3	18	0	0	0	7.0
[12]		5	3	15	12	6	0	7.2
[13]		3	6	12	0	0	0	6.0
[14]		3	1	9	12	2	0	8.0
[15]		17	1	48	0	12	0	3.6
[16]		3	1	24	0	6	0	10.3
[17]		3	1	28	0	0	3	10.7
[18]	(a) four-level	4	3	18	0	4	0	6.3
	(b) five-level	5	3	24	0	4	0	6.2
	(c) six-level	6	5	30	0	6	0	6.8
[19]		12	1	144	0	35	3	15.2
[20]		5	3	36	0	9	0	9.6
[21]	(a) the half-bridge based cell	3	1	12	0	6	0	6.3
	(b) the full-bridge based cell	5	1	24	0	6	0	6.2
	(c) the clamp-double	3	1	15	6	6	0	9.3
	(d) the three-level <i>FC</i>	3	1	12	0	6	0	6.3
	(e) the three-level <i>NPC</i>	3	1	12	6	6	0	8.3
	(f) the five-level cross-connected <i>SM</i>	9	1	36	0	12	0	5.4
[22]	(a) Mixed commutation cells	4	1	18	0	6	0	6.3
	(b) Asymmetrical commutation cells	4	1	18	0	6	0	6.3
	(c) Cross connected commutation cells	5	1	24	0	6	0	6.2
	(d) Clamped double commutation cells	4	1	15	6	6	0	7.0
	(e) T-connected <i>NPC</i> using <i>RB</i> switch	3	1	12	0	6	0	6.3
	(f) Alternative Active 3-L <i>NPC</i>	3	1	18	0	6	0	8.3
[24]	Hybrid <i>MLIs</i> topologies	6	7	30	0	0	0	6.2
[25]		7	8	36	6	0	0	7.1
[26]		6	13	30	0	0	0	7.2
[27]		3	4	12	0	0	0	5.3
[28]		3	6	12	0	0	0	6.0
[29]		4	3	11	20	0	0	8.5
[30]		5	3	18	24	6	0	10.2
[31]		5	6	24	0	0	0	6.0
[32]		5	6	24	0	0	0	6.0

Table I shows the computed ($F_{C/L}$) factor for the conventional types of the multilevel inverters and the introduced topologies in [11]–[22], [24]–[32]. From this table, it is clear that the topology presented in [15] records the lowest value for this factor and so it requires the smallest count of the components to produce the same voltage level number.

II. PROPOSED MODULAR MLI

A new modular three-phase *MLI* with reduced components count is proposed and studied in this paper. The suggested three-phase symmetrical inverter is shown in Fig. 1(a). Each arm consists of series connection of basic cells with a series connected switch, for example arm A consists of one cell connected in series with switch Q_1 . Adding the common dc voltage source (E) in to each arm forms the pole, creating the pole voltages (V_{A0}, V_{B0}, V_{C0}). In order to obtain the zero state pole voltage another switch Q_2 is added to the pole, similarly Q_4 and Q_6 for pole (B) and (C). Fig. 1(b) shows the primary basic cell, where each cell consists of two switches S_1, S_2 and single dc voltage source. The two switches operate in a complementary fashion. Therefore, each cell can produce two voltage levels ($0, E$): when S_1 in ON-STATE, zero voltage is produced across the cell terminals, and when S_2 in ON-STATE, E volt is applied across the cell terminals. Furthermore, using only one cell per each pole and applying suitable control signals to the S_1, S_2, Q_1 and Q_2 , three voltage levels per pole (i.e., $0, E, 2E$), are

produced. The output pole voltage for n cells connected in series configuration is shown in Fig. 1(c).

Table II summarizes the different switching states and the corresponding output voltages for both the basic cell and the pole voltage (V_{A0}) of the proposed *MLI* topology.

The proposed topology is a modular type therefore it can be extended to any levels. Equations (2)–(5) provide the relations of the proposed topology as

$$N_{Pole} = N_{Cell} + 2 \quad (2)$$

$$M_{Level} = 2N_{Cell} + 3 \quad (3)$$

$$N_{SW} = 3(2N_{Cell} + 2) \quad (4)$$

$$N_{PS} = 3N_{Cell} + 1. \quad (5)$$

Then for the example of $N_{Cell} = 1$, $N_{Pole} = 3$ [based on (2)] which is the pole voltage levels and $M_{Level} = 5$ [based on (3)] which is the output line-to-line voltage levels. Note that the number of output phase voltage levels N_{Ph} will be derived to be seven levels in low frequency modulation and nine levels for high frequency modulation.

III. MODULATION TECHNIQUES FOR THE PROPOSED MLI

The *MLI* modulation techniques are classified into two main groups according to the switching frequency used to

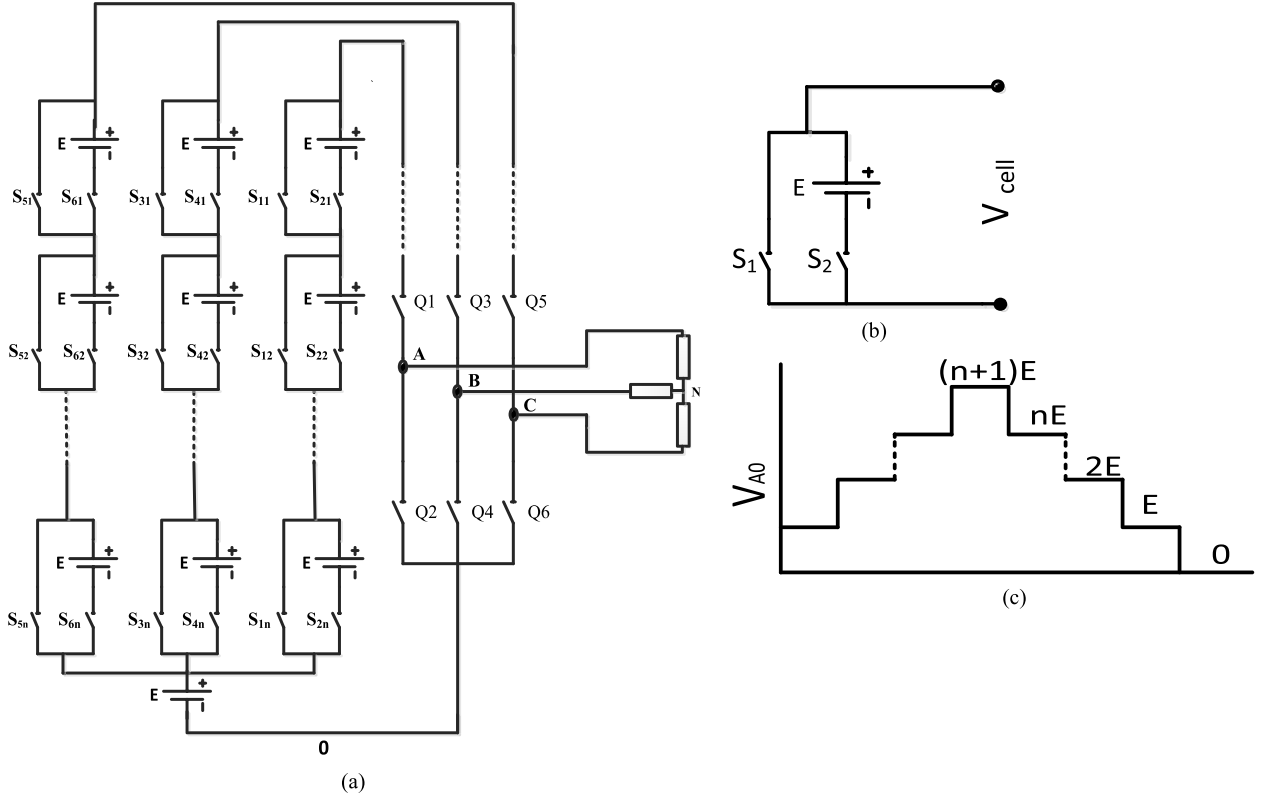


Fig. 1. (a) Generalized power circuit of the suggested three-phase symmetrical MLI. (b) Basic cell. (c) Pole voltage (V_{A0}) waveform for n -cell.

TABLE II
DIFFERENT SWITCHING STATES AND THE CORRESPONDING OUTPUT VOLTAGES

Switching states	Switch				Basic-unit Output voltage	Pole voltage (V_{A0})
	S_1	S_2	Q_1	Q_2		
1	ON	OFF	ON	OFF	0	E
2	OFF	ON	ON	OFF	E	$2E$
3	OFF	OFF	OFF	ON	-	0

drive inverter switches: 1) low frequency modulation technique, 2) pulse-width modulation (*PWM*) techniques that cover conventional *PWM* techniques, sinusoidal pulse-width modulation (*SPWM*), space vector pulse-width modulation (*SVPWM*), sub-harmonic pulse-width modulation (*SH - PWM*), and switching frequency optimal pulse-width modulation (*SFO - PWM*) [34]. In this paper, two modulation techniques are investigated to achieve sinusoidal output voltages waveforms as described in the following.

A. Low Frequency Modulation Technique

The low frequency modulation is considered as the basic modulation technique due to its lower switching frequency than the other modulation methods. It causes the switching losses reduced dramatically [33]. In order to investigate the performance of the proposed *MLI*, a three levels per pole by using single basic cell in each pole is used as shown in Fig. 2. It is simulated via PSIM and MATLAB/SIMULINK software packages. In order to generate the required switching signals for the proposed *MLI*, a rectified sine waveform has a frequency equals to the output voltage frequency ($=50$ Hz) is compared

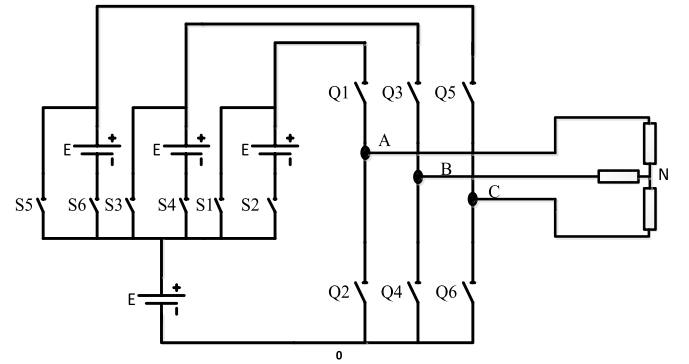


Fig. 2. Proposed three-phase MLI topology.

with a dc voltage signal has an amplitude equal to half of the sine wave amplitude as shown in Fig. 3. The intersection points between them identify six periods (P_1 to P_6).

Four switching signals are constructed from these periods combination in order to generate a sinusoidal output voltage. The control equations for the (S_1, S_2, Q_1 , and Q_2) are given in (6)–(9), respectively. The same scenario is applied to inverter

TABLE III
SWITCHING STATES OF THE PROPOSED TOPOLOGY (SWITCH ON: 1, S WITCH OFF: 0)

V_{AB}	V_{BC}	V_{CA}	S_1	S_2	Q_1	Q_2	S_3	S_4	Q_3	Q_4	S_5	S_6	Q_5	Q_6
E	$-2E$	E	1	0	1	0	0	0	0	1	0	1	1	0
$2E$	$-2E$	0	0	1	1	0	0	0	0	1	0	1	1	0
$2E$	$-E$	$-E$	0	1	1	0	0	0	0	1	1	0	1	0
$2E$	0	$-2E$	0	1	1	0	0	0	0	1	0	0	0	1
E	E	$-2E$	0	1	1	0	1	0	1	0	0	0	0	1
0	$2E$	$-2E$	0	1	1	0	0	1	1	0	0	0	0	1
$-E$	$2E$	$-E$	1	0	1	0	0	1	1	0	0	0	0	1
$-2E$	$2E$	0	0	0	0	1	0	1	1	0	0	0	0	1
$-2E$	E	E	0	0	0	1	0	1	1	0	1	0	1	0
$-2E$	0	$2E$	0	0	0	1	0	1	1	0	0	1	1	0
$-E$	$-E$	$2E$	0	0	0	1	1	0	1	0	0	1	1	0

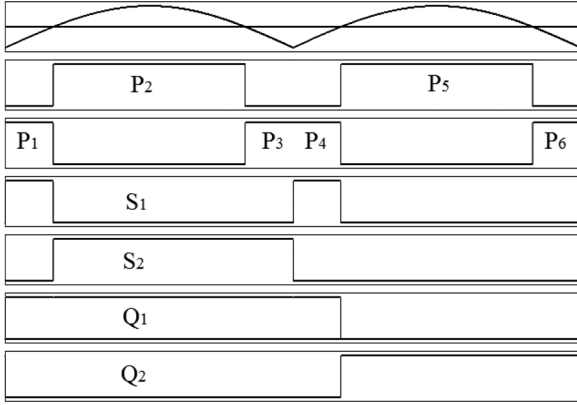


Fig. 3. Switching patterns for low frequency modulation technique.

poles (V_{B0}) and (V_{C0}) after shifting the basic sinusoidal voltage with -120° , 120° , respectively.

Therefore, the required switching signals for the overall three poles can be generated

$$S_1 = P_1 + P_4 \quad (6)$$

$$S_2 = P_2 + P_3 \quad (7)$$

$$Q_1 = P_1 + P_2 + P_3 + P_4 \quad (8)$$

$$Q_2 = P_5 + P_6 \quad (9)$$

where (+) stands to logic OR.

Balancing three phase output voltage can be achieved by operating the *MLI* according to switching states shown in Table III. The suggested *MLI* has 12 modes of operation per one cycle. It is essentially to note that: when switches Q_1 , Q_3 , and Q_5 are in OFF-STATE, switches S_1 to S_6 have two possibilities for operation. Switches S_1 to S_6 may be in ON-STATE or at OFF-STATE. Both of them will not affect the output waveforms. However, keeping switches S_1 to S_6 in the OFF-STATE will reduce the overall voltage stresses on Q_1 , Q_3 , and Q_5 .

B. Sinusoidal Pulse-Width Modulation Technique (SPWM)

The straight way to generate the *SPWM* signals is to compare a sinusoidal waveform signal with a triangular waveform. The comparison operation will produce the Boolean signals that are required to synthesize the switches control pulses. The *SPWM* technique is successfully applied for the proposed topology. Two different approaches have been proposed as follows.

1) *Scheme I: SPWM Using Single Carrier Signal*: This scheme uses one carrier signal centered with the sinusoidal modulation signal (sine waveform), and it has an amplitude equal to peak-to-peak value of the modulation signals as shown in Fig. 4. It worth mentioning that the modulation signal is shifted by dc level equals to $(CR/2)$, where CR is the carrier signal amplitude. The resulted Boolean output from the comparison between the carrier and the modulating signal produces the main pulse signal G_1 . Also the pulse signal GP_1 is generated by comparing the modulating signal with zero value. After logical processing on G_1 and GP_1 , the switching pulses S_1 , S_2 , Q_1 , and Q_2 can be generated as specified in (10)–(13)

$$S_1 = (G_1 \times \overline{GP_1}) + (\overline{G_1} \times GP_1) \quad (10)$$

$$S_2 = (G_1 \times GP_1) \quad (11)$$

$$Q_1 = GP_1 + \{(G_1 \times \overline{GP_1}) + (\overline{G_1} \times GP_1)\} \quad (12)$$

$$Q_2 = \overline{\{GP_1 \times (\overline{G_1} \times \overline{GP_1})\}} \quad (13)$$

where ($\times$) stands for logic AND, (+) stands for logic OR, ($-$) stands for invert, and S_1 , S_2 , Q_1 , Q_2 are the signals which will be applied to the gates drive belong to switches S_1 , S_2 , Q_1 , Q_2 , respectively. In order to avoid dc-power sources short circuit, (S_1 , S_2) and (Q_1 and Q_2) operate in a complementary mode with dead time.

2) *Scheme II: SPWM Using Two Carrier Signals*: This scheme compares single modulating signal with two identical and shifted in level carrier signals. Both of them have amplitude equal the modulating signal peak. In addition, the carrier signals are shifted by a dc offset equals to the carrier signal amplitude (CR_1) as shown in Fig. 5. Using the same procedure followed

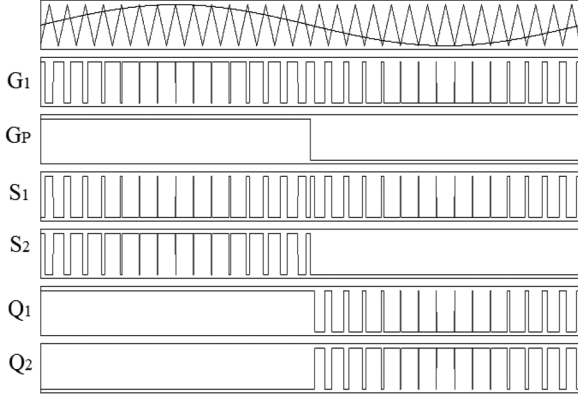


Fig. 4. Switching patterns of the proposed MLI for scheme I.

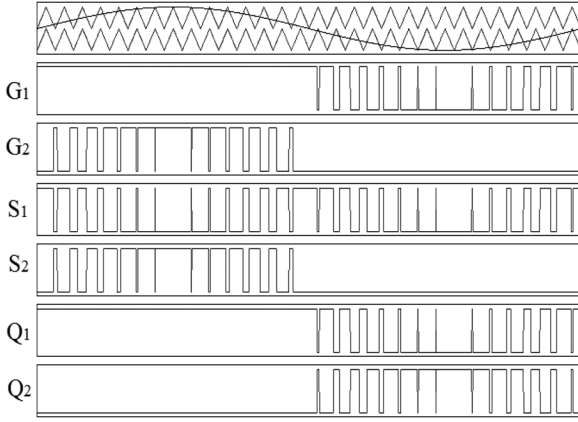


Fig. 5. Switching patterns of the proposed MLI for scheme II.

in scheme I, scheme II can be executed. However, due to using two carrier signals, there are two Boolean signals named G_1 and G_2 resulted from the comparison. By Carrying out several logical operations on these two signals (G_1, G_2) as given in (14)–(17), the required control pulses for MLI can be obtained

$$S_1 = (G_1 \times \overline{G_2}) \quad (14)$$

$$S_2 = G_2 \quad (15)$$

$$Q_1 = \overline{G_2} \times \overline{(G_1 \times \overline{G_2})} \quad (16)$$

$$Q_2 = \overline{G_2} \times (G_1 \times \overline{G_2}). \quad (17)$$

IV. SIMULATION AND EXPERIMENTAL RESULTS

The proposed topology has been simulated using MATLAB/PSIM software package tools. A single cell ($N_{\text{Cells}} = 1$) has been chosen to produce five levels per line-to-line load voltages according to (3). However, the proposed topology can be extended to n cells. The prototype of the proposed MLI is implemented and setup using the metal–oxide–semiconductor field-effect transistor (MOSFET) as switching devices and symmetrical dc-power supplies. For PWM implementation, the switching frequency is selected to be $f_s = 2.5$ kHz.

The proposed MLI prototype has been experimentally tested and compared with the simulation results. The DSP of type TMS320F28335 is used to generate the switching signals.

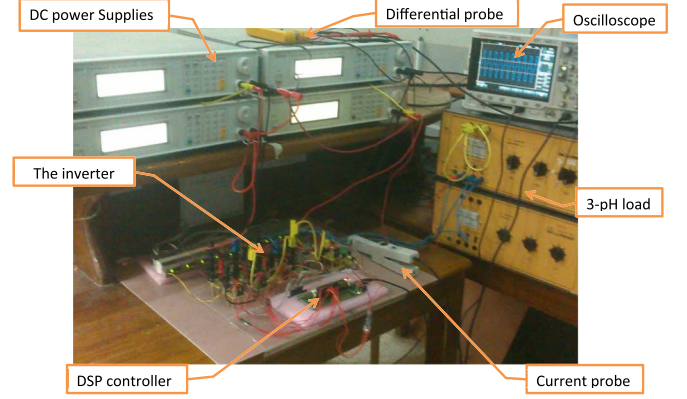


Fig. 6. Experimental setup of the proposed MLI.

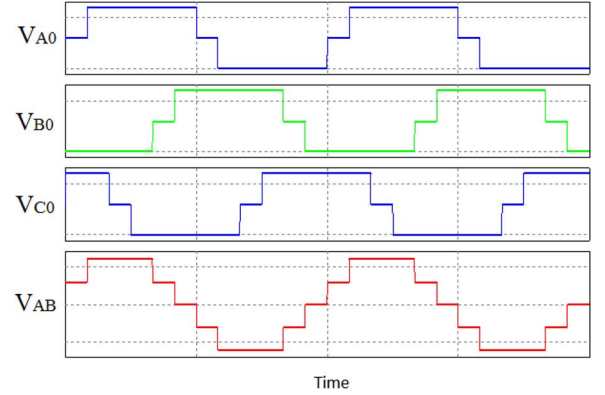
Fig. 7. Pole voltages (V_{A0}, V_{B0}, V_{C0}) and line-to-line voltage (V_{AB}) with low frequency modulation technique.

Fig. 6 shows the prototype setup used for the proposed MLI, which includes four dc-power supplies, switching devices, measurement tools, the DSP controller and three-phase resistive load. This section demonstrates the control flexibility of the proposed MLI based on low frequency modulation technique and the SPWM explained previously without loss of modularity.

The key element in the generation of the output voltages waveforms is the pole voltages (V_{A0}, V_{B0} , and V_{C0}). Each one of them is shifted by 120° in order to generate balanced three phase sinusoidal output voltages. The three pole voltages are shown in Fig. 7. The nonzero part determines the number of the utilized sources. Conventionally, generating the negative parts in the output voltage needs an H-bridge and as a direct result, the number of the used switches is increased. However, the proposed topology benefits from the zero part in the pole voltages waveform to produce the positive and negative parts in the output voltages waveforms. It achieved by subtracts each pole voltage with the neighboring one to produce the line voltage (as an example: $V_{AB} = V_{A0} - V_{B0}$) as in [13], [14], and [28].

The pole voltages waveform to produce the positive and negative parts in the output voltages as in [13], [14] and [28].

According to switching states provided in Table III, the suggested MLI produces three phase balancing line voltages as shown in Fig. 8, each line voltage has five levels and has a phase shift of 120° between each other. Also,

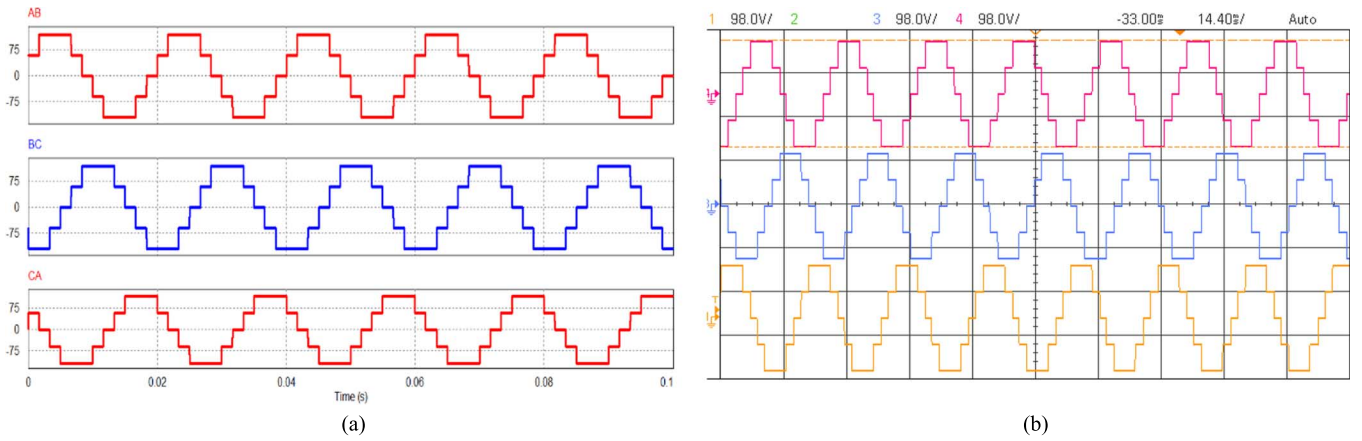


Fig. 8. Output line-to-line voltages (V_{AB} , V_{BC} , and V_{CA}) with low frequency (50 Hz) modulation technique. (a) Simulation. (b) Experimental.

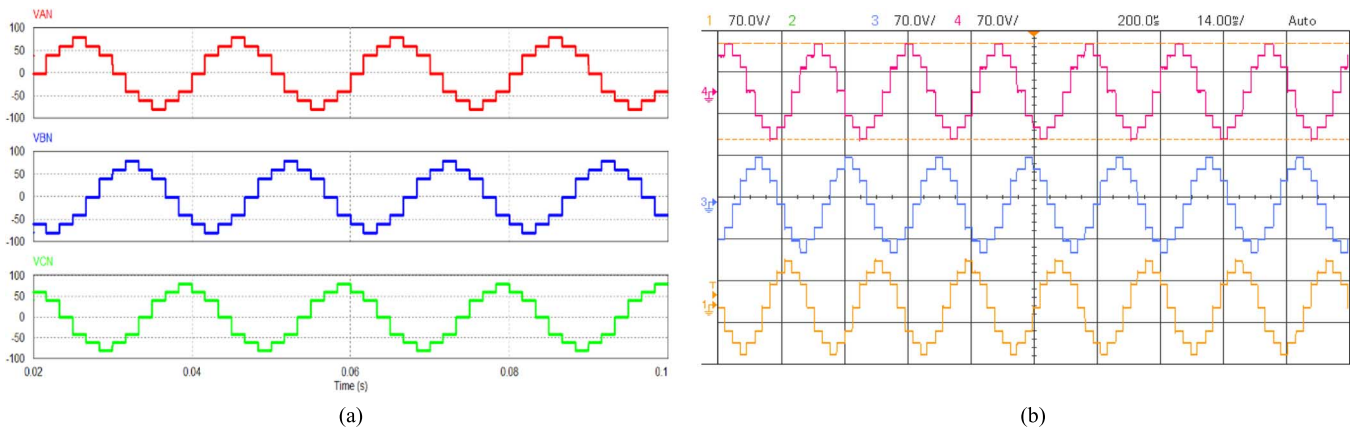


Fig. 9. Output phase voltages (V_{AN} , V_{BN} , and V_{CN}) with low frequency modulation technique. (a) Simulation. (b) Experimental.

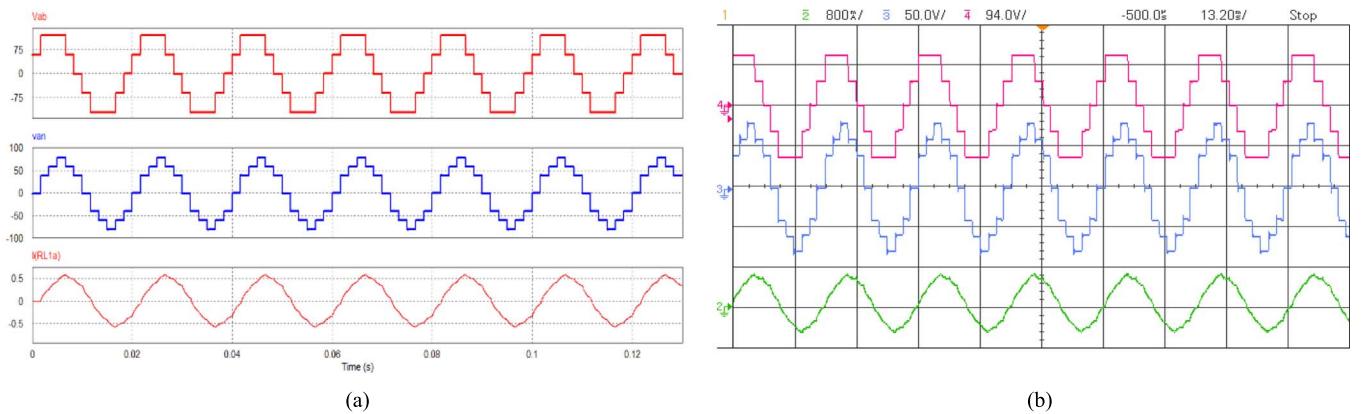


Fig. 10. Inverter outputs with $R-L$ load (V_{AB} , V_{AN} , and I_{AN}) with low frequency modulation technique. (a) Simulation. (b) Experimental.

as the pole voltages (N_{Pole}) have three voltage levels (0, E , $2E$ volts), the output line-to-line voltages (M_{levels}) have five voltages level ($2E$, E , 0 , $-E$, $-2E$ volts). The phase voltages (N_{phase}) are deduced from the pole voltages: they produce seven levels on the output phase voltages i.e., (E , $(4/3)E$, $(2/3)E$, 0 , $-E$, $-(4/3)E$, $-(2/3)E$ volts). The simulation and experimental results of the output phase voltage are shown in Fig. 9. In order to test the performance of the proposed MLI with low switching frequency, Fig. 10 shows the load line-to-line voltage, phase voltage and the phase current of

the proposed MLI when loaded by $R-L$ load ($R = 146$ ohm, $L = 73$ mH). Moreover, the performance of the proposed MLI has been tested using SPWM based on schemes I and II. Figs. 11, 12, and 13 demonstrate the pole voltage, output line-to-line voltages, and output phase voltage using Scheme I. Moreover, Figs. 14, 15, and 16 demonstrate pole voltages, output line-to-line voltages, and output phase voltage using Scheme II. It is notable that switching signals for S_1 , S_2 cannot operate simultaneously; the same criteria are applied to the Q_1 and Q_2 . Due to the hybrid switching frequency appeared in

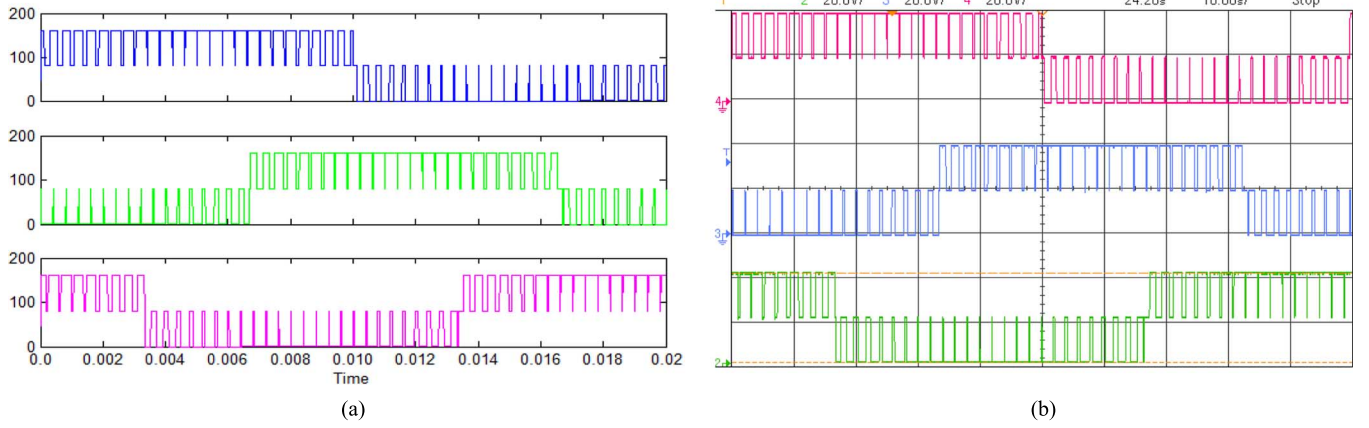


Fig. 11. Pole voltages for scheme I, $m_i = 0.95$ and $f_s = 2.5$ kHz. (a) Simulation. (b) Experimental.

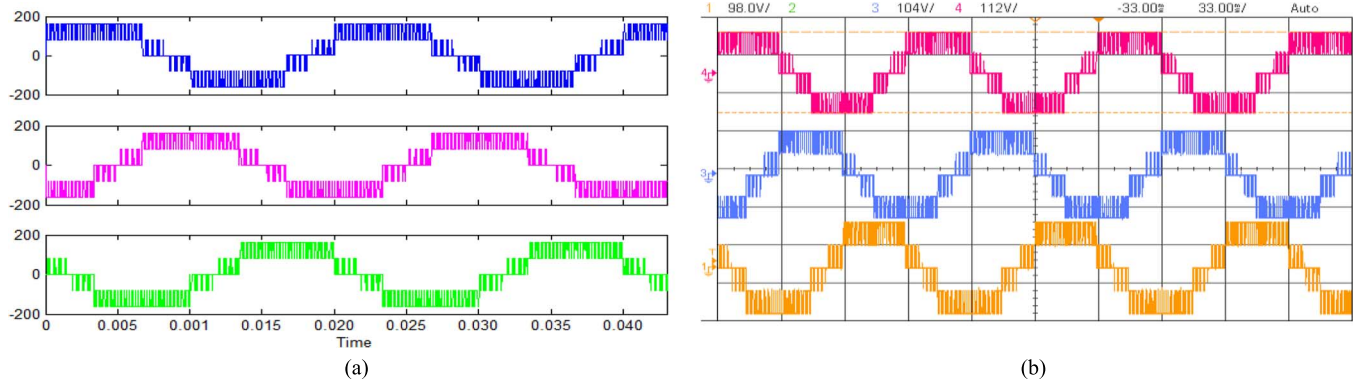


Fig. 12. Line-to-line voltages for scheme I, $m_i = 0.95$ and $f_s = 2.5$ kHz. (a) Simulation. (b) Experimental.

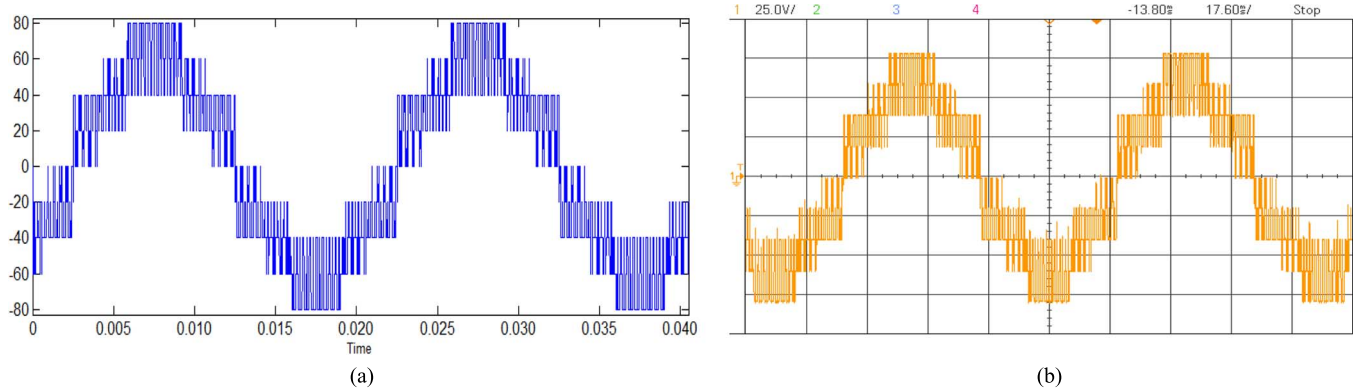


Fig. 13. Phase voltages for scheme I, $m_i = 0.95$ and $f_s = 2.5$ kHz. (a) Simulation. (b) Experimental.

switching signals for S_2 , Q_1 and Q_2 , the switching losses are expected to be reduced.

Since scheme I uses only one carrier signal compared to the modulating signal, the number of the output voltage levels (nine levels per phase voltages, five levels per line voltages) maintains their values even if the modulation index is decreased. This is shown in Figs. 13 and 17. However in scheme II, the output voltage levels is directly affected with the modulation index (m_i): When the modulation index is less than 0.5, the number of output voltage levels is (five levels per phase voltages, three levels per line voltages). However, when m_i is greater than 0.5,

number of output voltage levels become (nine levels per phase voltages, five levels per line voltages). This shown in Fig. 16, Fig. 18.

Moreover, the three phase output line-to-line voltages (V_{AB}, V_{BC}, V_{CA}), and (V_{AB}, V_{AN}, I_{AN}) at load terminals after the filter (filter components $L = 0.5$ mH, $C = 20$ μ F) are shown in Fig. 19. Fig. 20 presents the Total harmonic distortions (THD) of the three executed switching modulation schemes. The low frequency modulation scheme has the best THD among the three modulation techniques; it is about 16.88%. However, $SPWM$ will be more suitable for the

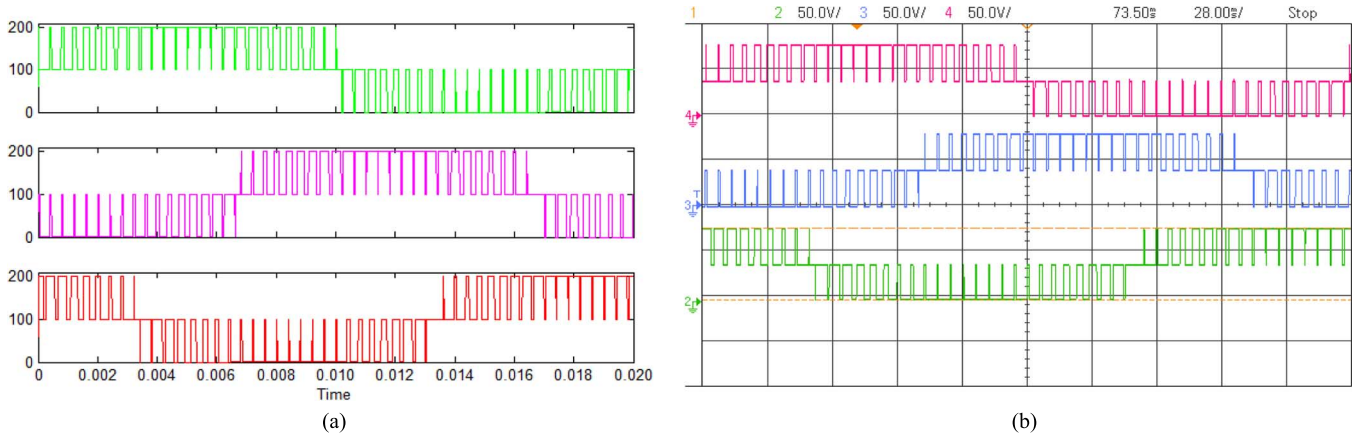


Fig. 14. Pole voltages for scheme II, $m_i = 0.95$ and $f_s = 2.5$ kHz. (a) Simulation. (b) Experimental.

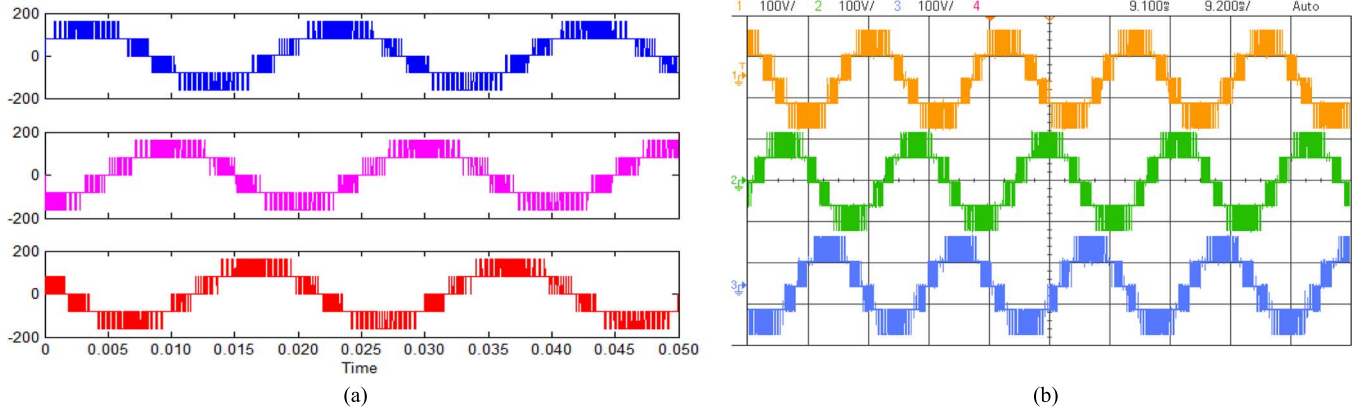


Fig. 15. Line-to-line voltages for scheme II, $m_i = 0.95$ and $f_s = 2.5$ kHz. (a) Simulation. (b) Experimental.

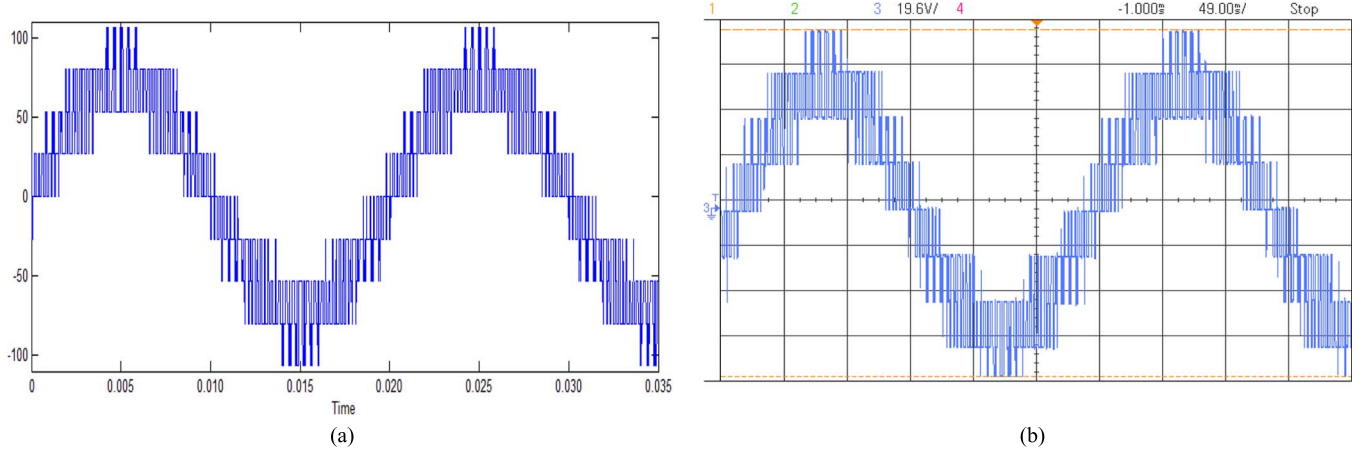


Fig. 16. Phase voltages for scheme II, $m_i = 0.95$ and $f_s = 2.5$ kHz. (a) Simulation. (b) Experimental.

closed loop operation and also strongly expected to minimize the harmonic contents of the inverter output voltage than low frequency modulation after the filter.

In order to ensure the feasibility of the proposed MLI, it is compared with the *MLI* topologies listed in [11]–[22], [24]–[32]. The comparison is based on the proposed factor introduced in the introduction ($F_{C/L}$). Table IV shows the main features of the proposed *MLI* compared to other inverters listed in Table I. Also, the three phase unsymmetrical topologies presented in the literature have been modified to be symmetrical in order to unify the base for our comparison. In

addition, any single-phase topologies listed in Table I have been modified to be matched with the other three phase topologies. The graphical representation of the comparison between the suggested topology and the presented topologies in [11]–[22], [24]–[32] is shown in Fig. 21.

Almost all the addressed topologies have components per level factors between “5” and “7”. The presented topology in [15], which has the lowest $F_{C/L}$ which equals to “3.6”, is utilizing single dc-power source to generate the required output voltage levels. It suffers from several disadvantages, such as using electrolyte capacitors that will increase the inverter foot-

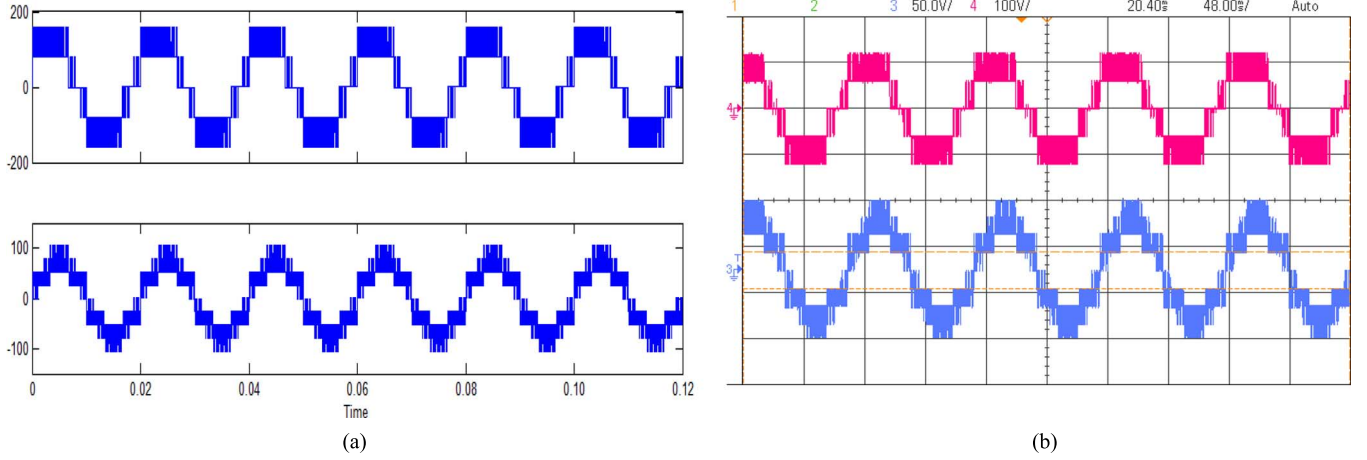


Fig. 17. Line-to-line voltage and phase voltage at for scheme I, $m_i = 0.5$ and $f_s = 2.5$ kHz. (a) Simulation. (b) Experimental.

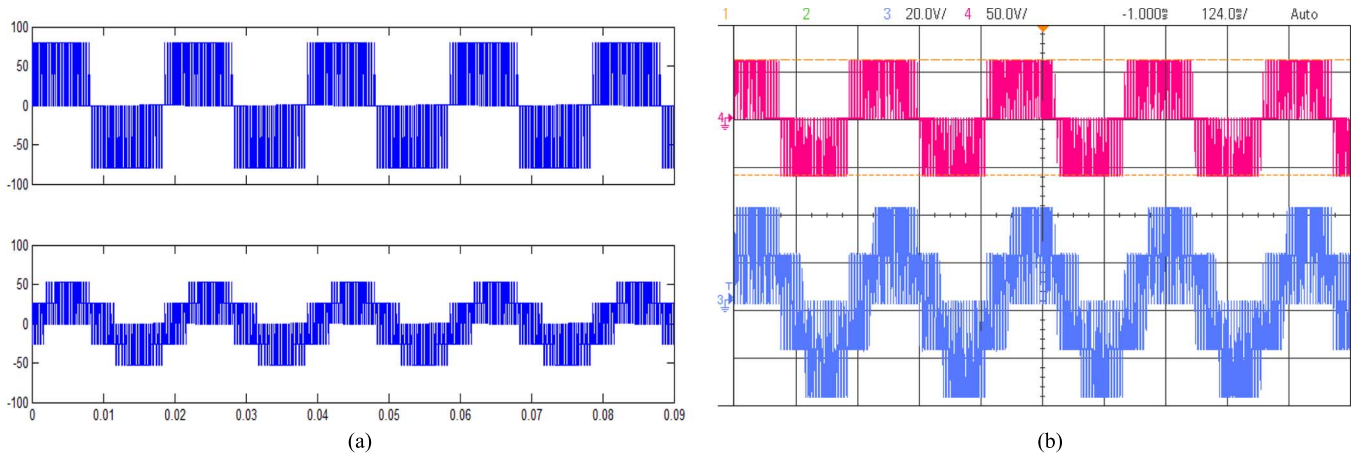


Fig. 18. Line-to-line voltage and phase voltage for scheme II, $m_i = 0.5$ and $f_s = 2.5$ kHz. (a) Simulation. (b) Experimental.

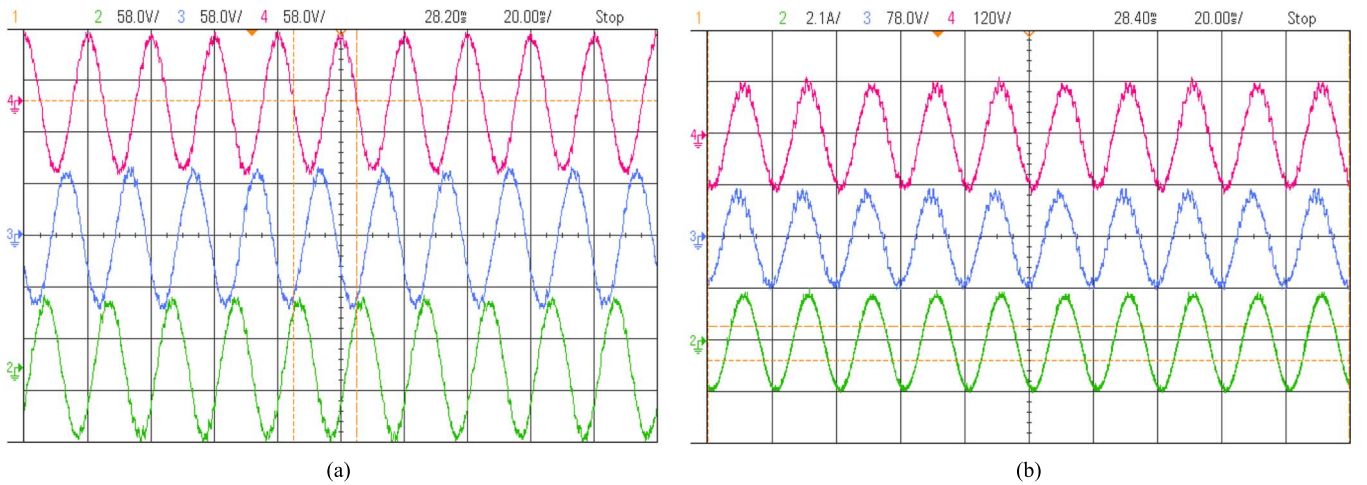


Fig. 19. Inverter output voltages: (a) three phase line-to-line voltages (V_{AB} , V_{BC} , and V_{CA}), (b) line-to-line voltage, phase voltage and the phase current under $R - L$ load.

print, reduce the inverter life time, and special control techniques are required for balancing capacitors voltages. In addition, this topology actually maximizes the output voltage levels number by controlling capacitors voltages to be fixed asymmetrical voltage values. Therefore, the function of the controller does not only have to keep constant equal voltages on the dif-

ferent capacitors but also it should maintain different voltages values across these capacitors. Hence, the reduction in power stage components that reflects low $F_{C/L}$ has been replaced by an extremely complicated control circuitry and algorithm. On the other hand, both [21] and [27] have similar performance factors $F_{C/L}$. The topology presented in [21] also suffering from

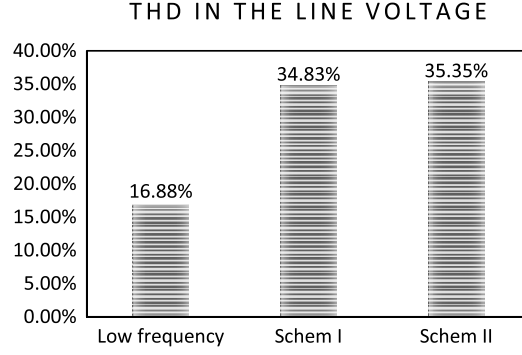


Fig. 20. Voltage total harmonic distortions (THD) with different modulation strategies.

TABLE IV
MLI PROPOSED TOPOLOGY

Proposed	N_{pole}	N_{PS}	N_{SW}	N_D	N_C	N_{tsf}	$F_{C/L}$
	3	4	12	0	0	0	5.3

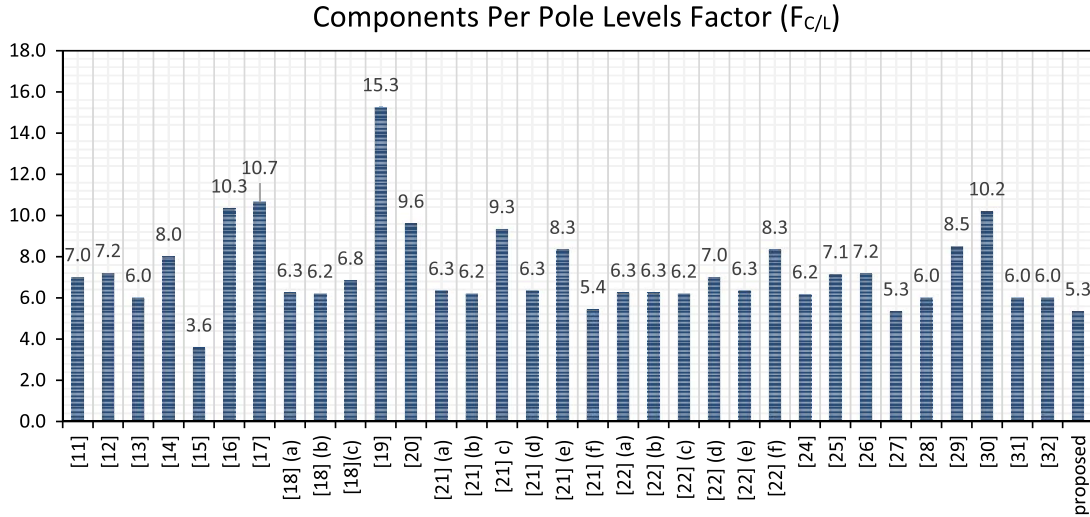


Fig. 21. Comparison between the proposed and the addressed topologies.

the presence of the floating power supplies (electrolytic capacitors) and its limitations that have been presented in the previous statements. Furthermore, both [21] and [27] have a shared disadvantage related to power losses in the inverter power stage: in other words, the zero-voltage across the inverter pole voltage, which essentially required in the pole voltage waveform, accomplished by allowing half of the used power switches per pole be in ON-STATE to conduct the load current. Therefore the conduction losses will increase intensively as the number of levels is increased. Thus, as a result, it is expected that the inverter efficiency will decrease. However, the proposed topology compared to the presented topologies provides a good solution from both system topology and control algorithm point of view. The problematic issues related to electrolytes capacitors and their voltages balancing have been eliminated. In addition, the path of load current has been shorted to pass through minimum power switches during zero voltage across the inverter pole. Therefore, the proposed inverter has better efficiency than the others.

V. CONCLUSION

A new modular multilevel inverter ($MMLI$) topology using two modulation control techniques is presented. The proposed MLI has several advantages compared with existing $MLIs$ topologies. A lower number of components count such as isolated dc-power supplies, switching devices, electrolyte capacitors, and power diodes are required. So it exhibits the merits of high efficiency, lower cost, simplified control algorithm, smaller inverter's foot print and increased the overall system reliability. Due to the modularity of the presented topology, it can be extended to higher stages number leads to a good performance issues such as low dv/dt , low EMI , and low THD and eliminating the output filter will be obtained. Beside the low frequency modulation, two $SPWM$ schemes are successfully applied to control the suggested MLI . This paper also suggests a significant factor $F_{C/L}$, which defines the required components to generate one voltage level across the output pole terminals.

The issue related to the cost of each used component is out of scope of this paper. The system simulation model and its control algorithm are developed using PSIM and MATLAB software package tools to validate the proposed *MLI* topology. A laboratory prototype has been developed and tested for various modulation indexes to verify the control techniques and performance of the topology, the similarity between the simulation and obtained experimental results was confirmed.

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